METHOD AND CIRCUIT FOR OFF CHIP DRIVER CONTROL, AND MEMORY DEVICE USING SAME

ABSTRACT OF THE DISCLOSURE

An off chip driver impedance adjustment circuit includes a storage circuit adapted to receive and store a drive strength adjustment word. A counter circuit is coupled to the storage circuit to receive the drive strength adjustment word and develops a drive strength count responsive to the drive strength adjustment word. A programmable fuse code to preset the counter. An output driver circuit is coupled to the counter circuit to receive the drive strength count and is adapted to receive a data signal. The output driver circuit develops an output signal on an output responsive to the data signal and adjusts a drive strength as a function of the drive strength count.